REMARKS

Present Status of the Application

The drawings are objected under 37 CFR 1.84(p)(5). The abstract of the disclosure is objected to and correction is required. The Office Action rejected all presently-pending claims 1-9. Specifically, the Office Action rejected claims 1-9 under 35 U.S.C. 103(a), as being unpatentable over Shimoda; Kenji et al. (U.S. 5404248) in view of Lahmeyer; Charles R (U.S. 4649541 A). The Office Action also rejected claims 1-9 under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 5-10 of U.S. Patent No. US 6662335 B1 in view of Roth; Ron M. et al. (U.S. 5719884 A). Applicants have amended a drawing and agreed to sign the terminal disclaimer to overcome double patenting. After entry of the foregoing amendments, claims 1-9 remain pending in the present application, and reconsideration of those claims is respectfully requested.

Discussion of Objections

The drawings are objected under 37 CFR 1.84(p)(5). In response thereto, Figure 1 is amended. The amended portion is that main data segment with reference number "130" is amended from "MAIN DATA 172 BYTES (D_{1880}~D_{2047})" to "MAIN DATA **168** BYTES (D_{1880}~D_{2047})." The reference number "116" in line 8 of page 2 is changed into "130." Since the data stored in the main data segment 130 is D_{1880}~D_{2047}, which is 168 bytes, instead of 172 Bytes. It is corrected to clarify the inconsistence of the disclosure and the corresponding figure.

The specification is amended to incorporate the description regarding the reference numbers "112", "114" and "116." The amendments are supported in the Figure 1.

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The Abstract of the disclosure is objected to and correction is required. In response thereto, Abstract of the specification is amended to meet the requirement.

It is believed that the foregoing amendments add no new matter to the present application. The amendments made to the Figure, Specification and Abstract are believed to overcome the Examiner's Objections.

Discussion of Office Action Rejections

The Office Action rejected claims 1-9 under 35 U.S.C. 103(a), as being unpatentable over Shimoda; Kenji et al. (U.S. 5404248, "Shimoda" hereinafter) in view of Lahmeyer; Charles R (U.S. 4649541 A, "Lahmeyer" hereinafter). Applicants respectfully traverse the rejections for at least the reasons set forth below.

It is well established at law that, for a proper rejection of a claim under 35 U.S.C. §103 as being obvious based upon a combination of references, the cited combination of references must disclose, teach, or suggest, **either implicitly or explicitly**, all elements of the claim at issue. Independent claims 1 and 7 are allowable for at least the reason that the Shimoda and the Lahmeyer, **either implicitly or explicitly**, do not disclose, teach, or suggest the feature of "a

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second decoder, for reading the error detection codes from the memory, **storing the error detection codes into a second buffer other than the memory**, and performing a second decoding on the data stored in the memory **when the data stored in the memory is sufficient to be assembled as a complete data block**" as defined in claim 1, and the Shimoda and the Lahmeyer, **either implicitly or explicitly**, do not disclose, teach, or suggest the feature of "a first decoder, for performing a first decoding to the row data stored in the first buffer and generating decoded data, **the decoded data is stored into a memory different from the buffer**, the decoded data is also sent to an error detection code generator, the error detection code generator generates the error detection codes for the decoded data, the generated error detection codes are stored into the memory", as defined in claim 7.

It is asserted that the disclosure of the Shimoda reference in view of the "RAM and One of Three Selectors 30" in the Lahmeyer can render claims 1 and 7 obvious. However, the "RAM and One of Three Selectors 30" in the Lahmeyer is different from that of the invention. As described in the Col. 5, Lines 11-22 of the Lahmeyer:

> "The use of a RAM interface with the input and output modules ***eliminates data transfer delays by keeping data in place in memory while switching access to moduls 42 and 48 as needed.*** The processing means operates on polynomials by passing them through FIFO outputs. This allows processing to begin on a second word before it is fully completed on a first word, and calculations are more direct. In addition, the dedicated hardware can operate at a higher clock rate than can programmed microprocessors, or a general purpose computer."

It is clear that the RAM disclosed in the Lahmeyer is used to store data while switching access to modules 42 and 48, which is different from "**storing the error detection codes into a**

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second buffer other than the memory" in claim 1 and also different from "storing **the decoded data into a memory different from the buffer**" in claim 7. The combination of Shimoda in view of Lahmeyer does not disclose, teach, or suggest the features that are highlighted in claim 1 above or that are highlighted in claim 7.

Further, none of the cited Shimoda and Lahmeyer's patents memtioned the feature "when the data stored in the memory is sufficient to be assembled as a compact data block," as defined in claim 1. Therefore, one of ordinary skill in the art would not be able to modify Shimoda and Lahmeyer to obtain all the technical features of the present invention.

For at least the foregoing reasons, Applicant respectfully submits that independent claims 1 and 7 patently define over the prior art references, and should be allowed. For at least the same reasons, dependent claims 2-6 and 8-9 patently define over the prior art as well.

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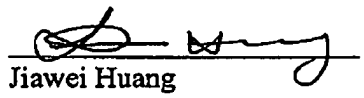
CONCLUSION

For at least the foregoing reasons, it is believed that the pending claims 1-9 are in proper condition for allowance. If the Examiner believes that a telephone conference would expedite the examination of the above-identified patent application, the Examiner is invited to call the undersigned.

Respectfully submitted,
J.C. PATENTS

Date: 10/29/2004



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